Electrical Instability of Double-Gate a-IGZO TFTs With Metal Source/Drain Recessed Electrodes

Gwanghyeon Baek, Linsen Bie, Katsumi Abe, Hideya Kumomi, and Jerzy Kanicki

***Abstract*— The electrical stability of double-gate (DG) and single-gate (SG) amorphous indium–gallium–zinc-oxide thin-film transistors (a-IGZO TFTs) with metal source/drain recessed electrodes on glass is investigated and compared. In the device structure of the a-IGZO TFTs, both top gate and bottom gate are defined by lithography, allowing independent or synchronized biasing. Bias temperature stress (BTS) are performed on SG a-IGZO TFTs and DG a-IGZO TFTs with synchronized gate bias condition. Under both positive and negative BTS, synchronized DG a-IGZO TFTs demonstrate much smaller ΔV_{TH} shift than SG a-IGZO TFTs.**

***Index Terms*— Amorphous indium–gallium–zinc-oxide (a-IGZO), bias temperature stress (BTS), double gate (DG), single gate (SG), thin-film transistor (TFT).**

I. Introduction

THERE is considerable interest in adapting amorphous InGaZnO thin-film transistors (a-IGZO TFTs) in such applications as active-matrix liquid crystal displays (AM-LCDs) [1] and active-matrix organic light-emitting displays (AM-OLEDs) [2]. This is because of its higher mobility in amorphous phase and suitability for low-temperature fabrication. We have previously shown [3] that the double-gate (DG) a-IGZO TFTs have better electrical and optical characteristics compared with the single-gate (SG) a-IGZO TFTs. However, to be adapted in the flat panel industry, its long term reliability must be ensured. Therefore, it is essential to evaluate the electrical stability of DG a-IGZO TFTs.

Although numerous results have been reported about the stability of SG a-IGZO TFTs [4]–[9], its microscopic origin and physical mechanism are still unknown. The a-IGZO TFT instabilities under positive-bias stress (PBS) have been explained by trapping in the gate dielectric [4], trapping in the bulk [8], or acceptor-like states creation [10], [11]. The last mechanism is supported by the parallel positive shift of the transfer characteristics observed during the PBS. The bulk donor state creation, on the other hand, is the basis of a quantities model recently proposed to explain negative bias stress in the presence of light [12], [13]. Still, there are only very few results related to the stability of DG a-IGZO TFTs. Abe *et al.* [14] reported the DG a-IGZO TFTs' instability when either top-gate (TG) or bottom-gate (BG) electrode is grounded. In either case, the stability of DG a-IGZO TFTs is no better than SG a-IGZO TFTs [14]. Previously, we have also shown [3], [15] that DG a-IGZO TFTs with the synchronized bias condition can produce larger current and steeper subthreshold swing in comparison with single BG (SBG) a-IGZO TFTs. Son *et al.* [16] reported the characteristics of the negative bias-temperature-stress (NBTS) for the synchronized DG a-IGZO TFTs. He has shown that the threshold voltage shifts (ΔV_{TH}) of the synchronized DG a-IGZO TFTs in the NBTS are lower than that of the SBG a-IGZO TFTs and concluded that the origin of this enhancement is due to the electric field compensation during the synchronized NBTS. The reduced ΔV_{TH} under the positive BTS (PBTS) are also reported. However, they did not explain the origin of this enhanced electrical stability.

In AM-LCDs, the TFT functions as a simple switch with a low duty cycle (0.1%), thus the TFT is under OFF-state for the 99.9% of the operation time. In other words, the gate voltage of the TFTs is lower than the voltages on the source and drain electrodes for most of the time. Therefore, the TFTs' characteristics under NBTS are important in the AM-LCDs. However, the threshold voltage shifts of a few volts can be tolerated in the AM-LCDs operation because the TFTs work as a simple switching element.

In contrast, in the pixel operation of the AM-OLEDs, the driving TFT (T_{DR}) is turned ON for most of time to supply the current on organic light emitting devices. In other words, the positive bias is always applied on the gate during T_{DR}. Moreover, a small threshold voltage variation on T_{DR} directly changes the driving current, resulting in pixel's brightness change. For example, Chen *et al.* [17] reported that a variation in threshold voltage (V_{TH}) of only 0.2 V changes the OLEDs brightness up to 10%. The PBTS instability, therefore, is critical for AM-OLEDs.

In this paper, we present the study of the PBTS and NBTS of DG a-IGZO TFTs with the synchronized bias condition. Furthermore, the instability results are compared with those of regular SBG TFTs. In the synchronized condition, the TG and BG electrodes are connected together, so same voltage is

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G. Baek, L. Bie, and J. Kanicki are with the Displays and Detectors Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA (e-mail: gbaek@umich.edu; lbie@umich.edu; kanicki@umich.edu).

K. Abe is with the Canon Research Center, Canon Inc., Tokyo 146-8501, Japan, and also with the Tokyo Institute of Technology, Kanagawa 226-0026, Japan (e-mail: k_abe@lucid.msl.titech.ac.jp).

H. Kumomi is with the Canon Research Center, Canon Inc., Tokyo 146-8501, Japan (e-mail: kumomi.hideya@canon.co.jp).

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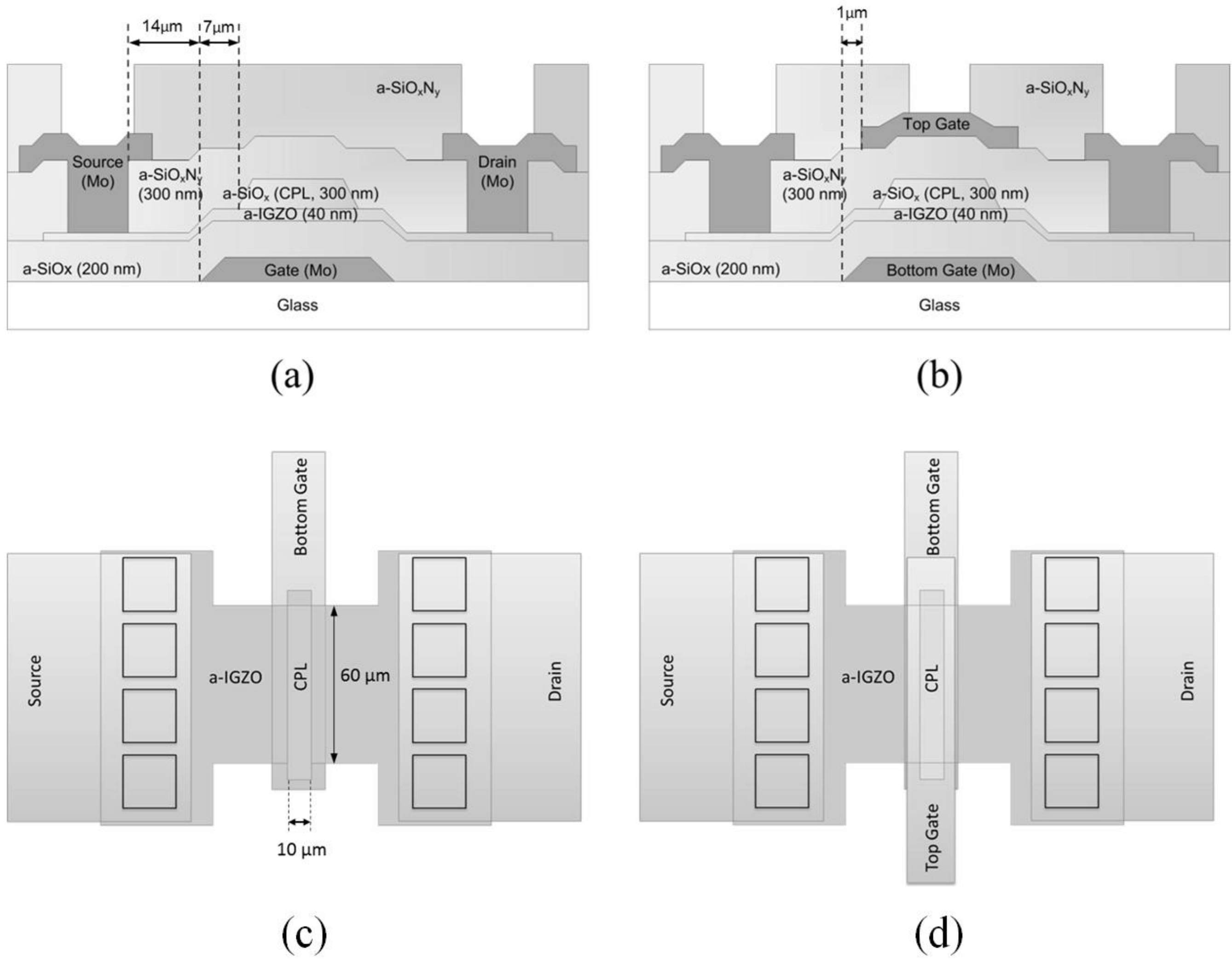

Fig. 1. Vertical structure of (a) SBG and (b) DG a-IGZO TFTs and top view structure of (c) SBG and (d) DG a-IGZO TFTs used for a stability study. The only difference between (a) and (c), and (b) and (d) is the existence of the TG electrode. The calculated C_{BG} and C_{TG} are 17.7 and 7 nF/cm^2, respectively. The channel width and length are 60 and 10 μm, respectively.

applied on both gate electrodes. This type of device structure does not need additional gate line, which is important in the pixel aperture optimization.

II. Device Structure

The a-IGZO TFTs with the metal source/drain (S/D) recessed electrodes are fabricated on a glass substrate (TFT grade glass). The cross sections and top views of the SBG and DG TFTs are shown in Fig. 1. In this structure, the amorphous silicon oxide (a-SiO$_x$) channel protection layer (CPL) deposited by plasma-enhanced chemical vapor deposition (PECVD) defines the TFT width W and Length L: $W = 60\ \mu$m and $L = 10\ \mu$m. On top of the CPL, a passivation layer (PL) of 300-nm-thick amorphous silicon nitride (a-SiN$_x$) is deposited by the PECVD. During the a-SiN$_x$ PECVD process, a-IGZO areas outside the CPL are heavily hydrogen doped and act as S/D regions [3]. It should be noticed that Mo metal gates and Mo S/D electrodes do not overlap. There is a separation of $\sim$20 μm between the CPL edge and S/D via edge. The only difference between DG a-IGZO TFTs and SG a-IGZO TFTs is the existence of TG electrode. The calculated BG insulator capacitor C_{BG} and TG insulator C_{TG} are 17.7 and 7 nF/cm^2, respectively. More details about processing are given in the Appendix.

III. Positive Bias-Temperature Stress

A. Experiment Conditions

The PBTS measurements are performed using HP 4156A semiconductor parameter analyzer in the dark-shielding box with the ambient air. The device temperature was regulated by a heated chuck, which is controlled by Signatone temperature controller with a precision of 0.1 °C. Before the measurement, the TFTs are placed on the heated chuck, which is set at the desired measurement temperature until the temperature controller displays the stable values. This is for ensuring the thermal equilibrium. We use $T_{\mathrm{STR}} = 80$ °C as our BTS test temperature as it is standard TFT used for BTS studies of a-Si:H TFTs. In addition, this temperature is of practical interest, since the temperature of the panel can increase, up to 60 °C–80 °C during operation [18], [19].

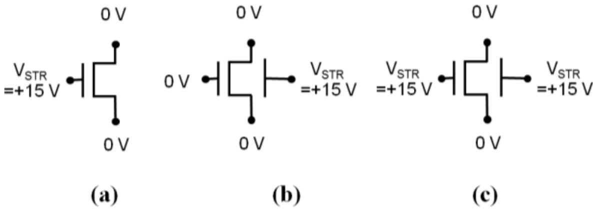

Fig. 2. PBTS setups for (a) SBG, (b) STG, and (c) DG TFTs (T_{STR} = 80 °C).

We selected a set of the SBG and DG TFTs for the comparison. The SBG and DG TFTs in the set are closely located, within 500 μm, on the substrate. The four sets over the 4-in glass substrate are measured to consider the process variation. For the SBG TFTs, the stress voltage of $V_{STR} = 15$ V is applied on the BG. To study the PBTS of single top-gate (STG) a-IGZO TFTs, similar V_{STR} is applied to the TG of one DG a-IGZO TFT in the set with bottom electrode grounded. For DG a-IGZO TFT with synchronized bias condition, stress voltage is applied to both TG and BG electrodes. During PBTS, the drain voltage is set to ground ($V_{DS} = 0$ V). These stress conditions for both device structures are illustrated in Fig. 2.

The TFTs are stressed for a total stress time of 10 000 s (2.78 h). At certain stress times (in log scale: 100, 300, 600, 1000, 3000, 6000, and 10 000 s), the stress are interrupted and the transfer characteristics are measured by sweeping the gate voltage (V_{GS}) at given stress temperature. To minimize a stress relaxation during these measurements, the measurement must be conducted as fast as possible. In this experiment, the measurement times of the transfer curves are below 10 s. This value is 10 times faster than the smallest stress interval, 100 s. To minimized the measurement time, the measurement accuracy is set to lower value and the range of voltage sweep are reduced, V_{GS} from −5 to 10 V. We believe that the reduced range is sufficient for investigation of the important TFT parameter, such as field-effect mobility, OFF current, subthreshold slope, and V_{TH}. Furthermore, we confirmed that the measured results for the range of $I_D > 10^{-11}$ A are not different with the data taken with a higher accuracy setup (but slow, longer than 50 s). All measured TFTs have the channel width and length of 60 and 10 μm, respectively.

B. Results and Discussion

Fig. 3 shows the transfer characteristics of the TFTs, measured during the bias stress at 80 °C ($V_{DS} = 0.1$ V). For all TFTs, the similar results are repeated on the same set and different set of devices, the observed results are reliable and reproducible. The threshold voltages (V_{TH}) are extracted from the transfer curves in Fig. 3. The best linear fitting method for 10%–90% of the maximum drain current is used for the V_{TH} extraction. The evolution of V_{TH}, ΔV_{TH}, is summarized in Fig. 5(a) with solid symbols. From Fig. 3, it is concluded that STG TFTs have a positive shift of $\Delta V_{TH} = 0.8$ V. DG a-IGZO TFTs showed smaller shift in the transfer curve ($\Delta V_{TH} = -0.3$ V) than the SG TFTs ($\Delta V_{TH} = -1.2$ V) under the PBTS.

It is worth noting that the transfer curves are shifting to the positive direction for STG a-IGZO TFTs [Fig. 3(b)], whereas

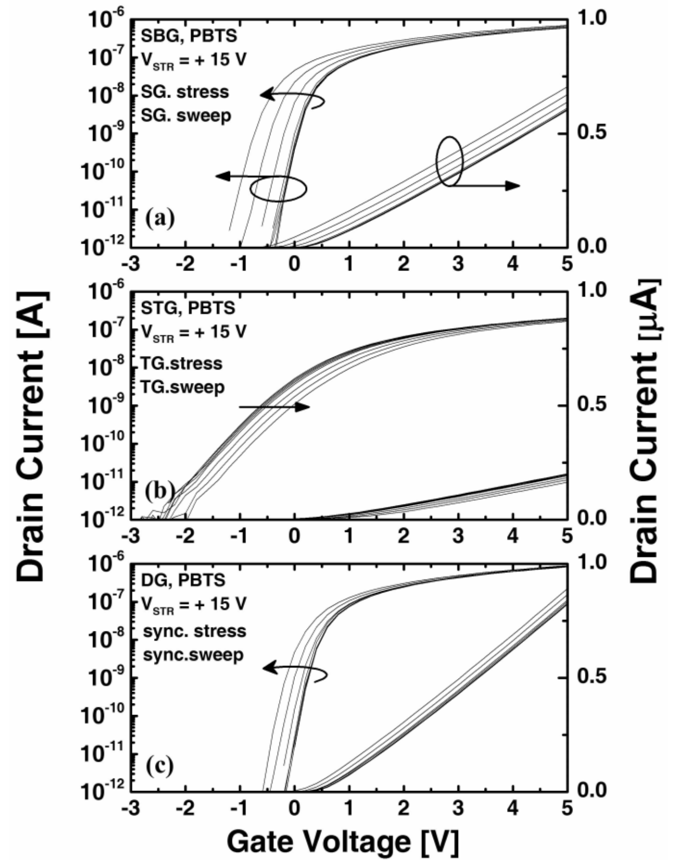

Fig. 3. Transfer characteristics of PBTS on (a) SBG, (b) STG, and (c) DG a-IGZO TFTs. Both SBG and double a-IGZO TFTs have negative V_{TH} shifts, whereas STG a-IGZO TFTs have positive shifts. The compared SG and DG TFTs are closely located within 500 μm (T_{STR} = 80 °C).

for both the SBG and DG a-IGZO TFTs, the shifts are negative [Fig. 3(a) and (c)]. In both cases, the changes in subthreshold swing and field effect mobility are negligible. However, the subthreshold slope of the STG a-IGZO TFTs (500 mV/decade) is much larger than SBG a-IGZO TFTs (170 mV/decade). It indicates that during the deposition of a-SiO_x CPL layer, larger number of oxygen vacancy defects is produced. These oxygen vacancies are then negatively charged during the PBTS and induce the positive shifts of the transfer curves. However, the observed negative ΔV_{TH} of DG and SBG a-IGZO TFTs cannot be explained by this mechanism. We are speculating that the reason of the negative shift can originate from electron tunneling from interface defects into the oxide conduction band and well down into the gate electrode, leaving behind positively charged defects inside a-SiO_x or at the interface with a-IGZO. These positive charges are responsible for the TFT negative threshold voltage shift.

As for the improved electrical instability in the synchronized DG a-IGZO TFTs compared with SG a-IGZO TFTs, there are two possible explanations: 1) increased effective gate capacitance, C_G, during the measurement of the transfer curves and 2) the vertical electric-field compensation. First, we expect that any change on C_G is expected to affect the TFTs transfer characteristics. If we assume that the bias stress induces the trapped charges near the interface of gate insulator and

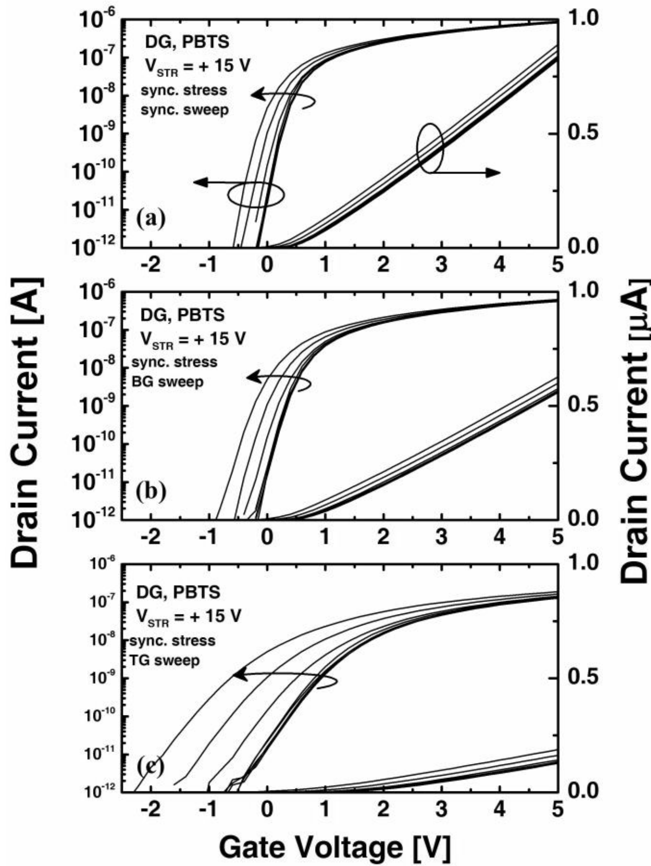

Fig. 4. Evolution of DG a-IGZO TFTs' transfer characteristics under the synchronized PBTS. V_{STR} of 15 V is applied on TG and BG. (a) Synchronized sweep. (b) BG sweep. (c) TG sweep. Although the same stress condition is used, the amounts of ΔV_{TH} are different with the readout (gate sweep) method.

semiconductor, the threshold voltage after the BTS (V_{TH}) and its shift (ΔV_{TH}) can be described by the following equations:

$$V_{TH} = V_{TH}(0) - \frac{Q}{C_G} \text{ and}$$
$$\Delta V_{TH} = V_{TH} - V_{TH}(0) = -\frac{Q}{C_G} \quad (1)$$

where $V_{TH}(0)$ is the threshold voltage of the fresh (unstressed) TFT. Q and C_G is the trapped charge amount near the interface and the gate capacitance of TFTs, respectively. From this equation, ΔV_{TH} is decreasing for the same Q when C_G has an increased value.

We confirmed previously [15] that the effective C_G of DG a-IGZO TFTs with synchronized bias ($V_{BG} = V_{TG}$) is equivalent to the sum of C_{BG} and C_{TG}. Therefore, C_G of DG a-IGZO TFTs ($C_{DG} = C_{BG} + C_{TG}$) is 24.7 nF/cm^2. In contrast, the effective C_G of SBG TFT is $C_{BG} = 17.7$ nF/cm^2. Furthermore, the DG a-IGZO TFT measured with BG sweep ($V_{TG} = 0$ V) or TG sweep ($V_{BG} = 0$ V) has an effective C_G equal to $C_{BG} = 17.7$ nF/cm^2 or $C_{TG} = 7$ nF/cm^2, respectively. According to (1) and from discussion above, ΔV_{TH} will have the lowest value for DG TFT with the synchronized bias measurement.

To verify the effective C_G impact on the TFT measurements, we measure ΔV_{TH} of the DG TFTs under different measurement conditions. While V_{STR} is applied to the both gate electrodes of the DG TFT during the stress time (i.e., synchronized stress), we measure the DG TFTs transfer curves under three different gate bias conditions (Fig. 4): 1) synchronized sweep; 2) BG sweep with $V_{TG} = 0$ V; and 3) TG sweep with $V_{BG} = 0$ V. The ΔV_{TH} extracted from Fig. 4 are summarized in Fig. 5(a). The DG TFT with synchronized sweep has a smaller ΔV_{TH} than the SG TFT. However, the DG TFT with the TG sweep shows a larger ΔV_{TH} then the SG TFT. It is evident from this paper that ΔV_{TH} is different when TFT is measured using different sweep methods even if the identical stress was applied to all TFTs.

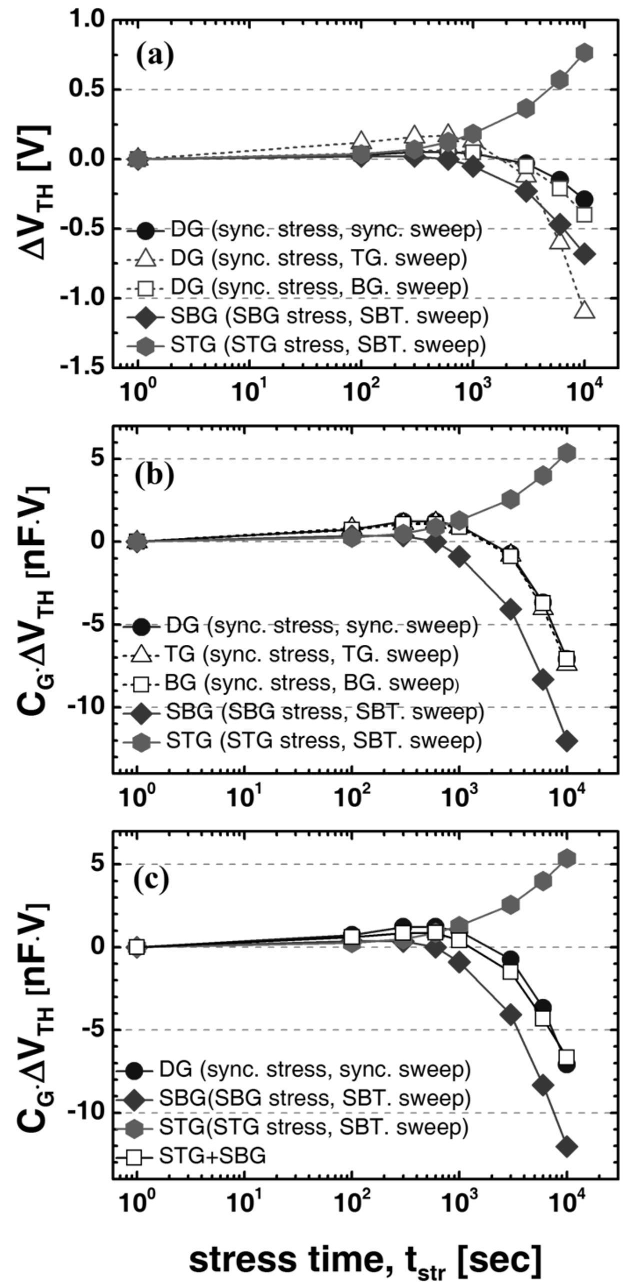

Fig. 5. Evolution of ΔV_{TH} under PBTS. (a) ΔV_{TH} versus stress time. (b) Gate capacitance normalized ΔV_{TH}, $C_G \cdot \Delta V_{TH}$. With the normalized ΔV_{TH}, the difference of the SG and DG a-IGZO TFTs is clearly distinguished. (c) Synchronized DG a-IGZO TFT PBTS result equals the sum of the SG a-IGZO TFT and STG a-IGZO TFTs PBTS result.

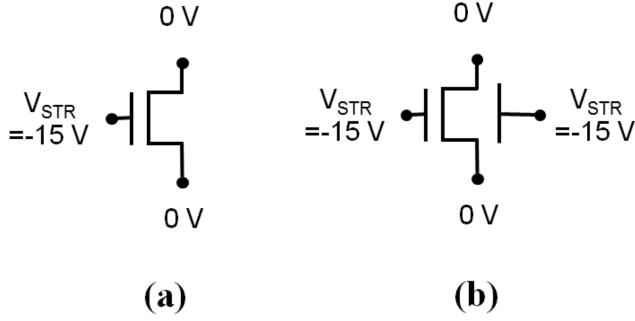

Fig. 6. NBTS setups for (a) SBG and (b) DG TFTs ($T_{STR} = 80$ °C).

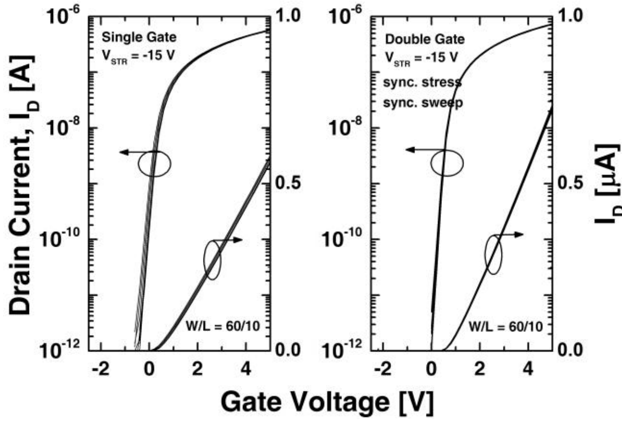

Fig. 7. Transfer characteristics during NBTS on SBG and DG a-IGZO TFTs.

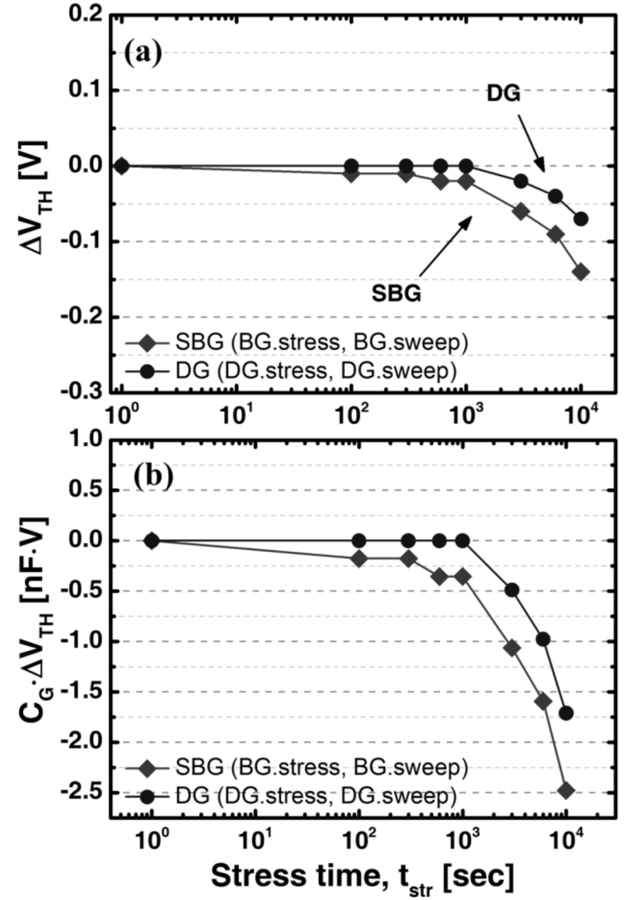

Fig. 8. Evolution of ΔV_{TH} under NBTS.$V_{STR} = -15$ V, $T_{STR} = 80$ °C, $W/L = 60/10$ (in micrometer). (a) ΔV_{TH} versus stress time. (b) Gate capacitance normalized ΔV_{TH}, $C_G \cdot \Delta V_{TH}$.

From experimental data shown in Fig. 5(a), we can observe that the magnitude of ΔV_{TH} is the largest for TG sweep and is the lowest for synchronized sweep. The effective C_G is the largest for synchronized sweep and the lowest for TG sweep. This is in agreement with (1). To avoid the C_G impact during transfer curve measurements, the ΔV_{TH} are normalized by multiplying C_G ($C_G \cdot \Delta V_{TH}$). This is shown in Fig. 5(b). It is clear that all three ΔV_{TH} curves are merged into the one curve after the normalization. Using the normalized ΔV_{TH}, we are now able to clearly establish the difference between SG and DG TFTs. Therefore, we recommend to use bias-induced charge Q ($C_G \cdot \Delta V_{TH}$) rather than ΔV_{TH}, when TFTs with different structures and under different measurement conditions are compared. Even after eliminating the C_G effects by the normalization, DG a-IGZO TFTs still shows smaller threshold voltage values than the SG TFTs [Fig. 5(b)].

Next, we consider the vertical field compensation in a-IGZO TFTs. The vertical field compensation in DG TFTs is understood as the vertical electric field induced by TG and BG cancel out each other, resulting in the zero or very small field being present in a-IGZO film. This would result a barely stressed a-IGZO film. However, during PBTS, the positive voltages on the gate electrodes will induce an accumulation of electrons in the a-IGZO channel. Furthermore, created electron accumulation layer will laterally connect source and drain electrodes, which are biased at 0 V. As a result, the mutual interaction between top and bottom electric fields is not allowed, and the vertical field compensation cannot take place during the PBTS.

To further investigate the origin of enhanced instability in DG a-IGZO TFTs, we take advantage of the normalization of ΔV_{TH} for different PBTS results. As shown in Fig. 5(c), the PBTS result of synchronized DG a-IGZO TFTs is the sum of instability of the SBG and STG a-IGZO TFTs. The better stability of the DG a-IGZO TFTs after normalization of ΔV_{TH} is the result of electron injection from the TG that neutralizes the positively charge defects at the BG a-SiO_x interface that were created during PBTS.

IV. Negative Bias-Temperature Stress

A. Experiment Conditions

The similar experiment is conducted for the NBTS. The measurement setups are shown in Fig. 6. The stress voltage of $V_{STR} = -15$ V is used.

B. Results and Discussions

The measured transfer curves are shown in Fig. 7 and the evolution of V_{TH} during the stress time are summarized in Fig. 8. For the SBG TFT, ΔV_{TH} is around -0.2 V and ΔV_{TH} smaller than -0.1 V are observed for DG a-IGZO TFTs under 80 °C. After Normalization, DG a-IGZO TFT still demonstrates a better instability than SG a-IGZO TFTs.

These observations are in a good agreement with the previously reported results in [16].

In contrast to the PBTS, during NBTS, the enhanced instability in DG a-IGZO TFTs could be explained by the vertical field compensation [3], [16]. For a negative gate bias, the hole accumulation layer is hardly formed in a-IGZO channel area. In other words, a-IGZO channel area is isolated from source and drain electrodes with high electrical resistance (lateral isolation). Consequently, a vertical interaction between the TG and BG electric field is allowed, resulting in the vertical field compensation in DG a-IGZO TFTs during NBTS. In other words, this will be equivalent to nearly zero bias stress across the a-IGZO channel region. Hence, it is expected that the interface electronic field and oxide field will be reduced during the NBTS. Therefore, as expected and in agreement with experimental results, we observe a very low ΔV_{TH} in DG TFTs during NBTS in comparison with SBG TFTs.

V. Conclusion

In this paper, the bias-temperature stability of the DG a-IGZO TFTs with the metal S/D recessed electrodes are investigated. The stress temperature is set to 80 °C and the stress time is 10 000 s. In PBTS with $V_{STR} = +15$ V, the ΔV_{TH} is reduced by one third in comparison with SBG TFTs. Similar experiments are performed for the NBTS with $V_{STR} = -15$ V. As well as in PBTS, the ΔV_{TH} of DG a-IGZO TFTs shows reduced values from that of the SBG. ($0.2 \rightarrow < 0.1$ V). From the results of this paper, we conclude that synchronized DG a-IGZO TFTs are more stable than the SBG a-IGZO TFTs under BTS and have great potential for the AM-FPDs pixel circuit.

Appendix

The process steps are described in the following. First of all, a 100-nm-thick Mo gate electrode is sputtered as a BG electrode and patterned by a dry etching using CF_4 and O_2 gases. Next, the PECVD is used for depositing the 200-nm-thick silicon oxide (SiO_x) as a BG insulator. ($C_{BG} = 17.7$ nF/cm^2). The substrate temperature (T_S) is set to 400 °C during the deposition and 24 sccm of silane (SiH_4) and 600 sccm of nitrous oxide (N_2O) are used. The 40-nm thick a-IGZO semiconductor film is dc deposited by oxygen (O_2) reactive sputtering (O_2/Ar $= 16.3/108.7$ sccm). The a-IGZO layer is patterned by a diluted hydrochloric acid (HCl) for 30 s. The dilution ratio is 10:1 (D.I. water:HCl).

The SiO_x CPL (300 nm) is deposited with a PECVD. To minimize hydrogen diffusion into a-IGZO channel, a lower SiH_4 and N_2O ratios (16/400 sccm) was used with T_s, set down to 285 °C. The CPL is dry etched with a gas mixture of CF_4 and O_2. The CPL defines a channel width and length of the fabricated TFTs.

Next, the CPL etching is followed by the first PL (1st PL) of silicon oxynitride (SiO_xN_y). Silicon oxynitride is known as a good moisture barrier [20]. The thickness of 1st PL is 300 nm. The PECVD deposition is used with gas mixture ratio of SiH_4:N_2O:N_2 = 24:30:570 sccm. Hence, the deposited film is nitrogen-rich SiO_xN_y. The pattering of the PL was done by dry etching through CF_4 and O_2 mixture. Next, the S/D contact vias and the TG electrode were sputtered over the 1st PL. (100-nm-thick Mo) The SG TFTs, used for the comparison, do not have the TG patterns in this step. The patterning of S/D contact was done by wet etching with Mo enchant (H_3PO_4:HNO_3:H_2O = 200:20:15, 20 s).

Additional passivation (2nd PL) is deposited by a 300-nm-thick SiO_xN_y, same condition as above, and patterned by wet etching [a low ammonium fluoride liquid (LAL 1000), for 90 s] to open contact area. The 2nd PL will allow an additional deposition of a transparent electrode (such as ITO), which can be used as a pixel electrode of AM-LCDs or AM-OLEDs. Finally, a thermal annealing was done using the rapid thermal annealing in nitrogen atmosphere, 300 °C for 30 min.

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Gwanghyeon Baek received the B.S. degree in physics from Korea University, the M.S. degree in electrical engineering from Seoul National University, and the Ph.D. degree in electrical engineering from University of Michigan, Ann Arbor, in 2002, 2004, and 2013, respectively. His current research interests include double gate a-InGaZnO TFTs and their application to active matrix imagers or displays. He is currently with Intel, Portland Technology Development.

Linsen Bie received the B.E. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2011, and the M.S. degree in electrical engineering from the University of Michigan, Ann Arbor, in 2013. He is currently with Apple, CA, as an Engineer.

Katsumi Abe received the B.S. and M.S. degrees in nuclear engineering from Kyoto University, Kyoto, Japan, in 1993 and 1995, respectively. He is currently pursuing the Ph.D. degree with the Tokyo Institute of Technology, Tokyo, Japan. He has been with the Canon Research Center, Canon Inc., Tokyo, Japan, since 2003. His current research interests include amorphous oxide semiconductor TFTs and their device physics.

Hideya Kumomi received the B.S., M.S., and Dr. Sci. degrees in physics from Waseda University, Tokyo, Japan. He has been with Canon Research Center, Canon Inc., Tokyo, for about two decades. His current research interests include nonlinear phenomena in phase transition, particularly on nucleation problems, and on TFTs based upon single-crystalline or polycrystalline Si and amorphous oxide semiconductors.

Jerzy Kanicki received D. Sc. from the Free University of Brussels, Belgium, in 1982. He joined the IBM T. J. Watson Research Center, as a Research Staff Member working on hydrogenated amorphous silicon devices for photovoltaic and flat panel display applications. In 1994 he joined the University of Michigan as a Professor in the Department of EECS. His current research interests include metal oxide semiconductors for displays and sensors.